REMARKS

Claims 1-15 are pending. Claims 1-15 are rejected under 35 U.S.C. §103(a). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

I. REJECTIONS UNDER 35 U.S.C. §103(a):

The Examiner has rejected claims 1-15 under 35 U.S.C. §103(a) as being unpatentable over Applicants' Background (pages 1, line 14 – page 4, line 22 of Applicants' Specification) in view of Bezzant et al. (U.S. Patent No. 6,014,717) (hereinafter "Bezzant"). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

A. Applicants' Background and Bezzant, taken singly or in combination, do not teach or suggest the following claim limitations.

Applicants respectfully assert that Applicants' Background and Bezzant, taken singly or in combination, do not teach or suggest "transmitting said payload of said received packet of data to said application whereby said application does not perform a lock, read, write or unlock operation on said transport control block" as recited in claim 1 and similarly in claims 6 and 11. The Examiner asserts that Bezzant teaches the above-cited claim limitation. Office Action (5/17/2007), page 3. Applicants respectfully traverse.

Bezzant instead teaches a PCMCIA host adapter includes the capability to master a non-DMA system bus and control a DMA data transfer between a DMA capable peripheral and the internal system memory. Abstract. Bezzant further teaches that a peripheral can be coupled to the system through a PCMCIA card plugged into a PCMCIA expansion slot. Abstract. Bezzant additionally teaches that a DMA controller coupled to the PCMCIA expansion slots through a PCMCIA bus controls a DMA transfer between the internal system memory and the peripheral. Abstract. Furthermore, Bezzant teaches that a bus master disables the CPU and takes control of the system bus during a DMA data transfer. Abstract.

There is no language in Bezzant that teaches transmitting the payload of a received packet of data. Neither is there any language in Bezzant that teaches transmitting the payload of a received packet of data to an application. Neither is there any language in Bezzant that teaches transmitting the payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation. Neither is there any language in Bezzant that teaches transmitting the payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation on the transport control block. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1, 6 and 11, since the Examiner is relying upon incorrect, factual predicates in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Claims 2-5 each recite combinations of features of independent claim 1, and hence claims 2-5 are patentable over Applicants' Background in view of Bezzant for at least the above-stated reasons that claim 1 is patentable over Applicants' Background in view of Bezzant.

Claims 7-10 each recite combinations of features of independent claim 6, and hence claims 7-10 are patentable over Applicants' Background in view of Bezzant for at least the above-stated reasons that claim 6 is patentable over Applicants' Background in view of Bezzant.

Claims 12-15 each recite combinations of features of independent claim 11, and hence claims 12-15 are patentable over Applicants' Background in view of Bezzant for at least the above-stated reasons that claim 11 is patentable over Applicants' Background in view of Bezzant.

As a result of the foregoing, Applicants respectfully assert that there are numerous claim limitations not taught or suggested in Applicants' Background in view of Bezzant, and thus the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1-15. M.P.E.P. §2143.

B. Examiner's motivation for modifying Applicants' Background with Bezzant to incorporate the missing claim limitations of claims 1, 6 and 11 is insufficient to establish a *prima facie* case of obviousness.

Most if not all inventions arise from a combination of old elements. *See In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Obviousness is determined from the vantage point of a hypothetical person having ordinary skill in the art to which the patent pertains. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Therefore, an Examiner may often find every element of a claimed invention in the prior art. *Id.* However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *See Id.* In order to establish a *prima facie* case of obviousness, the Examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). The Examiner must provide articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. *KSR International Co. v. Teleflex Inc.*, 82 U.S.P.Q.2d 1385, 1396 (U.S. 2007).

As understood by Applicants, the Examiner admits that Applicants' Background does not teach "transmitting said payload of said received packet of data to said application whereby said application does not perform a lock, read, write or unlock operation on said transport control block" as recited in claim 1 and similarly in claims 6 and 11. Office Action (5/17/2007), page 3. The Examiner asserts that Bezzant teaches the above-cited claim limitation. *Id.* The Examiner's motivation for modifying Applicants' Background with Bezzant to include the above-cited claim limitation is "so as to improve speed and reduce latency in transferring data." *Id.* The Examiner's motivation is insufficient to establish a *prima facie* case of obviousness in rejecting claims 1-15.

The Examiner has not provided any rational underpinning as to how the Examiner derived his motivation for modifying Applicants' Background to include the above-cited missing claim limitation. The Examiner simply states "so as to improve speed and reduce latency in transferring data" as motivation for modifying

Applicants' Background to include the above-cited claim limitation. While the Examiner may consider many factors in finding a reason to combine, the Examiner still must explain how the Examiner derived the motivation for modifying Applicants' Background to include the above-cited missing claim limitation. *KSR International Co. v. Teleflex Inc.*, 82 U.S.P.Q.2d 1385, 1396 (U.S. 2007). Applicants respectfully request the Examiner to point out how the Examiner derived the motivation for modifying Applicants' Background to include the above-cited missing claim limitation. The Examiner has not provided any evidence as to how the Examiner derived the motivation for modifying Applicants' Background to include the above-cited missing claim limitation. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 1-15. *Id.*

Further, the Examiner' motivation ("so as to improve speed and reduce latency in transferring data") does not provide reasons, as discussed further below, that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would modify Applicants' Background to include the above-indicated missing claim limitation of claims 1, 6 and 11. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-15. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

Why would the reason to modify Applicants' Background to transmit the payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation on the transport control block (missing claim limitation) be so as to improve speed and reduce latency in transferring data? What is the rationale connection between the Examiner's motivation (reducing latency in transferring data) and transmitting the payload of a received packet of data to an application whereby the application does not perform a lock, read, write or unlock operation on the transport control block (missing claim limitation)? Hence, the Examiner's motivation does not provide reasons that the skilled artisan, confronted with the same problems as the inventor and with no

knowledge of the claimed invention, would modify Applicants' Background to include the missing claim limitation of claims 1, 6 and 11. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1-15. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

II. CONCLUSION:

As a result of the foregoing, it is asserted by Applicants that claims 1-15 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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